



PATENT
450100-4465.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

18
7-19-03
Robert
Response

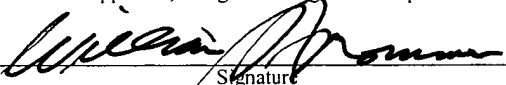
Applicant(s) : Takumi OKAUE et al.
Serial No. : 09/467,221
For : EXTERNAL STORAGE APPARATUS AND CONTROL
APPARATUS THEREOF, AND DATA TRANSMISSION RECEPTION
APPARATUS
Filed : December 20, 1999
Examiner : Ahshik Kim
Art Unit : 2876

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June 18, 2003

William S. Frommer, Reg. No. 25,506

Name of Applicant, Assignee or Registered Representative



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AMENDMENT

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Office Action mailed in the above-identified application on
March 18, 2003. In light of the remarks to follow, reconsideration and allowance of this
application are respectfully solicited.

Claims 19-24 remain in this application. In the Office Action under reply, the newly cited patent to Matsuo (U.S. Patent 5,974,513) was relied upon to reject claims 19 and 22 as allegedly being anticipated under 35 USC 102. Matsuo was combined with Robinson (U.S. Patent 5,388,248, cited previously) to reject claims 20 and 23 under 35 USC 103; and with Jigour (U.S. Patent 5,815,436, cited previously) to reject claims 21 and 24. However, as will now be described, Matsuo fails to suggest elements recited in each of claims 19 and 22; and for this reason, Matsuo fails to anticipate these claims. The deficiencies in Matsuo are not cured by Robinson and/or Jigour; and since claims 20-21 depend from claim 19, while claims 23-24 depend from claim 22, claims 20-21 and 23-24 are unobvious over the combinations of Matsuo and Robinson and Matsuo and Jigour.

Claim 19 recites, "a switch settable to a state which inhibits writing data into said flash memory." The Examiner takes the position that Matsuo describes a switch "such as 311" that, presumably, is settable to a write inhibit state (see section 2, page 2, line 24 of the Office Action). It is respectfully submitted that Matsuo does not show, suggest or describe a switch that is settable to a write inhibit state. Reference numeral 311 is used by Matsuo to describe a gate (see Fig. 2 and col. 3, lines 65-67 of Matsuo). The gate is included in a password address comparison circuit that produces a High output when power is applied to memory card 100 and a Low output if the external device with which the memory card is used supplies the correct address to the memory card. This correct address is the address at which a password is stored. When gate 311 produces a Low output, the stored password is read out from the semiconductor memory 2 of the memory card. It is seen, then, that gate 311 is not a *switch*, as recited in claim 19. The gate simply provides an output that is indicative of an address comparison.

Claim 19 also recites:

“control means for controlling said memory card in accordance with an instruction transmitted from said external apparatus, said control means *sending to said external apparatus* via said interface the *state of said switch in response to a read status instruction transmitted thereto via said interface from said external apparatus* and said control means *receiving from said external apparatus data to be written to said flash memory and a write instruction signal only if the state of said switch that is sent to said external apparatus is not said state which inhibits writing.*”

Matsuo fails to suggest such a “control means,” especially a control means having those elements emphasized above. In Matsuo, when power first is supplied to the memory card, the card enters a write inhibit state. This state is changed over to a write enable state if the external device with which the memory card is used sends the correct password to the memory card. Whether or not the password that is sent is correct is determined by comparing the password received from the external device with the password that is stored in the memory card. The password stored in the memory card is read out for this comparison operation by reading out the password that is stored in a predetermined memory location, namely, the memory location that is addressed by the external device.

There is nothing in Matsuo’s memory card that *responds to a read status instruction transmitted from the external apparatus*. This is not surprising, inasmuch as Matsuo does not send a *read status instruction* to his memory card. Although Matsuo sends a write control signal to the memory card, this write control signal is analogous to Applicants’ claimed “write instruction signal.” There is no *read status instruction* sent by Matsuo to his memory card.

Nor does Matsuo send to the external device *the state of said switch*. As mentioned previously, there is no switch in Matsuo, so it follows that there is no need to send the status of that missing switch to the external device. Clearly, there is no teaching or even a remote suggestion by Matsuo that the status of such a switch should be sent to the external device in response to receiving from that external device an instruction to read the status of that switch.

Even using the Examiner's erroneous characterization of Matsuo's gate 311 as a switch, the output of this gate *is not sent to the external device*. Rather, the output of gate 311 is used to read out the contents (i.e. the password) of an addressed memory location.

Finally, Matsuo does not describe the reception of data from the external device *only if the state of the switch is not the write inhibit state*. In fact, Matsuo does not describe whether data is *sent* to his memory card only if the memory card is in the write enable state. Presumably, data is sent from the external device to the memory card irrespective of the inhibit state of the memory card. Of course, that data is not written in the memory if the memory card is, in fact, in the write inhibit state. Nevertheless, there is nothing in Matsuo to suggest that if the memory card remains in its write inhibit state, data *is not* sent from external device 200 to memory card 100.

Claim 22 is directed to a system that includes the memory card of claim 19 in combination with the external apparatus that communicates with that memory card. The memory card recited in claim 22 is similar to the memory card of claim 19 in that the memory card of claim 22 includes:

“control means for controlling said memory card in accordance with an instruction transmitted from said external apparatus, said control means *sending to said external apparatus* via said interface the *state of said switch in response to a read status instruction transmitted* thereto via said interface *from said external apparatus* and said control means responding to a write instruction received from said external apparatus via said interface to write into said flash memory data received from said external apparatus;”

and the external apparatus of claim 22 includes:

“a controller for writing data to or erasing data from the flash memory of said memory card, said controller *transmitting a read status instruction* to said memory card via said interface *to determine whether a data writing operation* to the flash memory of said memory card *is inhibited* and said controller transmitting via said interface said write instruction and said data to be written into said flash memory *after said external apparatus receives said state* of said switch and *only if said state is not the state that inhibits writing*.”

Thus, claim 22 specifies those limitations that are not suggested in Matsuo: sending a read status instruction to the memory card from the external apparatus; sending to the external apparatus the state of the write-inhibit switch of the memory card; sending data to the memory card only after the state of the write-inhibit switch is received by the external apparatus and only if that state is not the inhibit state.

Therefore, since significant claim recitations are not found in Matsuo, it must be concluded that Matsuo does not anticipate claim 19 or claim 22. Moreover, there is nothing in Matsuo or in any of the other references cited by the Examiner that would suggest to one of ordinary skill in the art that Matsuo should be reconstructed in a manner that would render claims 19 and 22 obvious. The allowance of these claims is, therefore, respectfully solicited.

Claims 20 and 23 were rejected as being obvious in view of the combination of Matsuo and Robinson. Claim 20 depends from claim 19 and claim 23 depends from claim 22. Since these dependent claims include all of the limitations of the claims from which they depend, it follows that claims 20 and 23 are patentably distinct over Matsuo for those reasons that have been explained above. Robinson adds nothing to cure the aforementioned deficiencies of Matsuo. Robinson was cited for its teaching of several connectors (there are 41 such connectors) for connecting a flash memory card to other apparatus. Claims 20 and 23 recite “nine connectors.” The Examiner relies on the description of Robinson as meeting this recitation – admittedly, 41 connectors includes 9 connectors. But, Robinson does not suggest the aforequoted “control means” or “controller” recited by claims 19 and 22 and incorporated into claims 20 and 23. Accordingly, claims 20 and 23 are unobvious over the combination of Matsuo and Robinson; and the withdrawal of the rejection of these claims is respectfully requested.

Claims 21 and 24 were rejected as being obvious in view of the combination of Matsuo and Jigour. Claim 21 depends from claim 19 and claim 24 depends from claim 22. Since these dependent claims include all of the limitations of the claims from which they depend, it follows that claims 21 and 24 are patentably distinct over Matsuo for those reasons that have been explained above. Jigour adds nothing to cure the aforementioned deficiencies of Matsuo. Jigour was cited for its alleged teaching of the transmission of data in serial form. While claims 21 and 24 state that data is communicated in serial form between the memory card and the external apparatus, these claims, by reason of their dependencies, also recite the “control means” and “controller” of claims 19 and 22. Jigour is not suggestive of such control means or controller. Thus, even if Jigour is added to Matsuo, the resultant combination still does not teach sending a read status instruction to the memory card from the external apparatus; sending to the external apparatus the state of the write-inhibit switch of the memory card; and sending data to the memory card only after the state of the write-inhibit switch is received by the external apparatus and only if that state is not the inhibit state. Therefore, claims 21 and 24 are unobvious over the combination of Matsuo and Jigour. The rejection of these claims should be withdrawn.


Accordingly, claims 19-24, all the claims remaining in this application, are in condition for allowance. An early notice to this effect is respectfully requested.

Statements appearing above in respect to the disclosures in the cited references represent the present opinions of the undersigned attorney and, in the event the Examiner disagrees with any of such opinions, it is respectfully requested that the Examiner specifically indicate those portions of the references providing the basis for a contrary view.

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Respectfully submitted,
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WSF:lf